CLAIM AMENDMENTS

Please amend claims 1, 9, 17, and 21 as follows.

1. (Currently Amended) A method, comprising:

receiving a virtual page number lookup request at a virtual Translation Lookaside Buffer (TLB), wherein the virtual TLB includes an instruction TLB and a data TLB, wherein the TLB is configured to operate in a processor having an Xscale core architecture;

performing a lookup of the virtual page number in the virtual TLB, wherein performing the lookup of the virtual page number includes performing the lookup of the virtual page number in the instruction TLB and the data TLB simultaneously; and

returning a physical page number corresponding to the virtual page number in the virtual TLB.

2. (Canceled).

3. (Previously Presented) The method of claim 1, further comprising performing a page table lookup if a virtual address is not found in the virtual TLB.

4. (Original) The method of claim 3, further comprising updating the virtual TLB with the virtual page number and a corresponding physical page number resulting from the page table lookup.

5. (Original) The method of claim 4 wherein updating the virtual TLB includes:

updating the data TLB if a physical address corresponding to the virtual address has stored data; and

updating the instruction TLB if the physical address corresponding to the virtual address has stored an instruction.

6. (Original) The method of claim 4 wherein the virtual TLB is updated using a round robin algorithm.

7. (Original) The method of claim 3 wherein the page table lookup is performed by an operating system.

8. (Original) The method of claim 1 wherein the virtual page number lookup request is received from one of a Data Memory Management Unit (DMMU) or an Instruction Memory Management Unit (IMMU).

9. (Currently Amended) An apparatus, comprising:
a virtual Translation Lookaside Buffer (TLB) configured to operate in a processor having an Xscale core architecture, the virtual TLB including:

an instruction TLB and a data TLB; and

a TLB lookup logic coupled to the instruction TLB and the data TLB, wherein the TLB lookup logic is configured to lookup a virtual page number in the instruction TLB and the data TLB simultaneously.

10. (Previously Presented) The apparatus of claim 9 wherein the virtual TLB is configured to return a physical page number corresponding to the virtual page number if a virtual address is found in the instruction TLB or the data TLB.

11. (Original) The apparatus of claim 9 wherein the virtual TLB to report a TLB miss if the virtual page number is not found in the instruction TLB or if the virtual page number is not found in the data TLB.

12. (Previously Presented) The apparatus of claim 9, further comprising a machine-readable medium coupled to the virtual TLB, the machine-readable medium including instructions that, if executed, perform operations comprising:

receiving a TLB miss indicator from the virtual TLB; and

performing a page table lookup using a virtual address.

13. (Original) The apparatus of claim 12 wherein the machine-readable medium further includes instructions that, if executed, perform operations comprising:

providing the virtual TLB with the virtual page number and a corresponding physical page number resulting from the page table lookup.

14. (Original) The apparatus of claim 13 wherein the machine-readable medium further includes instructions that, if executed, perform operations comprising:

providing the data TLB with the virtual page number and the corresponding physical page number if a physical address corresponding to the virtual address has stored data; and

providing the instruction TLB with the virtual page number and the corresponding physical page number if the physical address corresponding to the virtual address has stored an instruction.

15. (Original) The apparatus of claim 13 wherein the virtual TLB is updated using a round robin algorithm.

16. (Original) The apparatus of claim 9 wherein the apparatus to execute instructions substantially in compliance with an Advanced RISC (Reduced Instruction Set Computer) Machines (ARM) instruction set.

17. (Currently Amended) A system, comprising:

a Dynamic Random Access Memory (DRAM) unit; and

a processor having an Xscale core architecture, the processor being coupled to the DRAM unit, the processor including:

a virtual Translation Lookaside Buffer (TLB), the virtual TLB including:

an instruction TLB and a data TLB; and

a TLB lookup logic coupled to the instruction TLB and the data TLB, wherein the TLB lookup logic is configured to lookup a virtual page number in the instruction TLB and the data TLB simultaneously.

18. (Previously Presented) The system of claim 17 wherein the virtual TLB is configured to return a physical page number corresponding to the virtual page number if the virtual page number is found in the instruction TLB or the data TLB.

19. (Previously Presented) The system of claim 17, further comprising a machine-readable medium coupled to the processor, the machine-readable medium including instructions that, if executed by the processor, perform operations comprising:

receiving a TLB miss indicator from the virtual TLB if the virtual page number is not found in the virtual TLB; and

performing a page table lookup in the DRAM unit using a virtual address.

20. (Original) The system of claim 19 wherein the machine-readable medium further includes instructions that, if executed by the processor, perform operations comprising:

providing the data TLB with the virtual page number and a corresponding physical page number if a physical address corresponding to the virtual address has stored data; and

providing the instruction TLB with the virtual page number and a corresponding physical page number if the physical address corresponding to the virtual address has stored an instruction.

21. (Currently Amended) An article of manufacture, comprising:

a machine-readable medium including instructions that, if executed by a machine, cause the machine to perform operations comprising:

receiving a virtual page number lookup request at a virtual Translation Lookaside Buffer (TLB), wherein the TLB is configured to operate in a processor having an Xscale core architecture, wherein the virtual TLB includes an instruction TLB and a data TLB;

performing a lookup of the virtual page number in the virtual TLB, wherein performing the lookup of the virtual page number includes performing the lookup of the virtual page number in the instruction TLB and the data TLB simultaneously; and

returning a physical page number corresponding to the virtual page number in the virtual TLB.

22. (Previously Presented) The article of manufacture of claim 21 wherein the machine-readable medium further includes instructions that, if executed by the machine, cause the machine to perform operations comprising:

performing a page table lookup if a virtual address is not found in the virtual TLB.

23. (Original) The article of manufacture of claim 22 wherein the machine-readable medium further includes instructions that, if executed by the machine, cause the machine to perform operations comprising:

updating the virtual TLB with the virtual page number and a corresponding physical page number resulting from the page table lookup.